

Arjun Hary

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OBJECTIVE

Seeking an Internship in Design / Verification for ASIC and FPGA domains

EDUCATION

University of Arizona, Tucson, AZ. (www.arizona.edu)

- Master of Science, Computer Engineering (currently pursuing)
- CGPA: 4/4

Government College of Technology, Coimbatore. TN, India. (www.gct.ac.in)

- Bachelor of Engineering in Electrical and Electronics Engineering, May 2006
- CGPA: 8.6/10

AREAS OF FOCUS

Embedded Systems,RTL design

EXPERIENCE

Jan 2007 - Present

Reconfigurable Computing Lab

Research Assistant

Working on the FPGA implementation of Non equispaced FFT. Identifying the kernel for Non equispaced FFT and mapping it to the FPGA for parallel implementation and speedup.

Dec 2007 - Present

University of Arizona

Graduate Assistant

Currently designing a Web application using PHP, MYSQL and AJAX for implementation of a simulation game in a medical context

June 2006 - July 2007

Cognizant Technologies Solutions Ltd., Chennai. TN, India. (www.cognizant.com)

Designation: Programmer Analyst Client: ACE Hardware

Project :Business Priorities Development (BPD)

- Developed ASP pages for the store system
- Developed COBOL and Mainframe programs for the retail system
- Designed and Developed online screens for Mainframe
- Other responsibilities included maintenance of DB2 and IMS databases and batch Job Scheduling

TECHNICAL SKILLS

Languages: Verilog, SystemC, C, C++, Web technologies(PHP, HTML, AJAX)

RTL Simulator: Xilinx ISE

OS: Unix (SVR4, Linux), Mac OS X, MS Windows XP/Vista

Tools/Lib.: Dreamweaver, SWISH, Photoshop, 3D studio MAX, PVCS

Assembly: MIPS, Intel 8085, 8086, 8051

Database: DB2, IMS, MYSQL

COURSEWORK

Reconfigurable Computing, Computer Aided Logic Design (RTL design) , Engineering of Computer based Systems(Embedded Systems) , Computer Architecture, Fundamentals of Computer Networks.

PROJECTS

[RTL Synthesis - Verilog]

- **I2C Bus Interface:** Simulated an I2C bus interface using Xilinx ISE involving a Temperature sensor, Memory and Master controller in Verilog
- Designed and Simulated Verilog code to find the count of number of occurrences of any given value in a Memory

[C, C++]

- **Logic Optimization tool:** Implemented Iterated Consensus, Row & Column Dominance and Branch & Bound algorithm as a Logic Optimization Tool in C
- **VPR:** Explored the effect of wirelength predictions at clustering stage to develop an initial placement to speedup the placement stage in the FPGA CAD flow.
- **Digital Speed control of a DC motor :** Implemented a C program to control the speed of a DC motor with a help of an Intel 8255 PPI.

[Assembly - 8051]-Undergraduate Final Project

- **Implementation of Synchronous Closing using Microcontroller:** The project uses the 8051 microcontroller with the help of a thyristor circuit to eliminate transients and control the switching of capacitor banks into the system which are used for power factor improvement.

