

**Adarsha Sreeramareddy**  
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### **Professional Interests**

- ❖ Reconfigurable systems
- ❖ Embedded system design
- ❖ Hardware Software co-design.

### **Work Experience**

#### **The University of Arizona**

**Research Assistant, Department of Electrical and Computer Engineering** **2007-2008**

##### **Partial Reconfiguration and Self-Healing**

- ❖ Part of Self-Configurable Architecture for Reusable Space Systems (SCARS), an ongoing NASA project.
- ❖ Use of Microblaze soft processor core to handle partial reconfiguration of a Virtex-5 FPGA for the purpose of self-healing systems.
- ❖ VHDL and C language used for development and coding.
- ❖ Tools used are Xilinx ISE, PlanAhead and Xilinx Embedded Development Kit.

##### **Research on Capacitance-Voltage variations in MOS devices with High-K dielectric films**

- ❖ Research was done in collaboration with the Department of Chemical Engineering.
- ❖ Involved CV Measurements and behavior of High-K dielectric layers in MOS devices.
- ❖ Done as part of the NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing.
- ❖ Measurements done using a Probe Station and LabVIEW virtual instrument.

##### **Two Level Boolean Logic Minimizer**

- ❖ Designed and implemented a two-level Boolean logic minimizer.
- ❖ Based on Quine McCluskey, Iterative Consensus methods.
- ❖ Coding was done in C language.

##### **I<sup>2</sup>C Bus Interface**

- ❖ Designed and simulated an I<sup>2</sup>C Bus Interface, to allow for communication between a Master Controller, Temperature Sensor and Memory.
- ❖ Design was done using Verilog HDL.
- ❖ Tools used were Xilinx ISE and the Xilinx ISE Simulator.

#### **Centre for Development of Advanced Computing, India**

**2006-2007**

##### **Intern**

- ❖ Designed and developed an AMBA AHB IP core to act as an interface between the LEON 3 core and an AES/DES encryption engine.
- ❖ Later implemented on a Virtex4 FPGA.
- ❖ AMBA AHB specifications were made use of and the code was written using VHDL.

## **Technical Expertise**

### **Operating Systems**

Windows (9X, 2000, ME, XP), MS-DOS.

### **Programming**

C, C++, VHDL, Verilog, Assembly level programming for 8085, 8086 and 8051, HTML, PHP, MYSQL, LDAP.

### **Software Tools**

Xilinx ISE, Xilinx Embedded Development Kit, ModelSim, Xilinx PlanAhead, LabVIEW, MATLAB, Code Composer Studio (CCS), Keil  $\mu$ Vision, Flash Magic, Tanner Tools (T-Spice, S-Edit, L-Edit, W-Edit), Dreamweaver.

### **Hardware Tools**

FPGA, CPLD, PGLA, DSP (TMS320C6713) kit, 8085, 8086 and 8051 kits.

## **Education**

- ❖ **Aug 2007 – Present** : Master of Science in Electrical and Computer Engineering, The University of Arizona  
**Advisor** : Dr. Ali Akoglu
- ❖ **Sep 2003 – June 2007** : Bachelor of Engineering in Electronics and Communication, Visveswaraiah Technological University, India

### **Major Courses in M S**

Reconfigurable Computing, Computer-Aided Logic Design, Computer Architecture and Design, Engineering of Computer-Based Systems, Fundamentals of Computer Networks.

## **Publications**

- ❖ Adarsha Sreeramareddy, Jeff G. Josiah, Ali Akoglu. "SCARS: Scalable Self-Configurable Architecture for Reusable Space Systems". The International Conference on Engineering of Reconfigurable Systems and Algorithms, July 14-17, 2008.

## **Activities, Memberships and Achievements**

- ❖ Research Assistant, 2007-present.
- ❖ Computer Support Student Worker (Web Developer), 2007-present.
- ❖ Member, IEEE Student Chapter, 2005-2007.
- ❖ Distinction Awards given by PES Institute of Technology, 8 semesters.
- ❖ 6-pointer Award given by the Council for the Indian Secondary Certificate Examination, 2001.