

ECE 506

Reconfigurable Computing

Fall 2008

Course Information

Class Hours: Mondays 3:30-6:00pm
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Office Hours: Mondays 10:00 AM – 11:00 AM, Wednesdays 2:00 PM – 3:00PM or by appointment
Course Page: <http://ece.arizona.edu/~ece506/>

Pre-requisites:

Digital design fundamentals, computer architecture and organization, programming language (C is a must, VHDL/Verilog knowledge preferred)

Text-book: Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation by Scott Hauck, André DeHon and other reading material will be either presented in the class or available as online papers.

Course Description

Scientific community has started exploring reconfigurable computing as a new and innovative technology for accelerating parallel computing. Today, in sheer density state-of-the-art reconfigurable devices are outpacing the microprocessor industry. Thus, they have the capability, especially aggregated on specially designed printed circuit boards, to become self-contained, high-end supercomputers. Moreover, their flexibility raises the possibility of meta-architecture; "morphing" hardware configurations with software as needed to improve efficiency, robustness, security and capability on-the-fly.

In this class, we investigate the state-of-the-art in reconfigurable computing both from a hardware and software perspective; understand both how to architect reconfigurable systems and how to apply them to solving challenging computational problems. The purpose of this course is to prepare students for engaging in research on reconfigurable computing.

Initially, we review in detail the basic building blocks of most reconfigurable computers. Characteristics of FPGA architecture such as the organization of device logic and interconnection resources are examined to quantify hardware limitations. These physical limitations are then contrasted with computer-aided design issues such as the selection of circuit component locations in devices (the placement problem) and subsequent circuit interconnection between components (the routing problem). While discrete FPGA devices offer an abundance of usable logic, most current reconfigurable computing applications require hardware configurations of multiple FPGAs and memory components organized in a computing system. We then focus on the architecture for existing multi-FPGA systems and on compilation techniques for mapping applications described in a hardware description language to reconfigurable hardware. **We will explore the question of “What makes an application suitable for reconfigurable computing” with case studies in Bioinformatics, Image processing, Video Processing, Cryptography, Molecular Dynamics and Computational Fluid Dynamics. We evaluate the FPGA based application acceleration with the emerging multicore architectures from the perspectives of price/performance and performance/watt.** Specific contemporary reconfigurable computing systems are examined to identify existing system limitations and to highlight opportunities for research in dynamic and partial configuration areas. Assignments will allow students to gain hands on experience in FPGA design cycle

and programming paradigms (verilog/hdl, mitrion-c). Semester long application and experimentation oriented project will give the students the opportunity to explore state of the art research topics in this field.

Topics Covered

- Introduction to Reconfigurable Computing (1 week)
- FPGA Architectures (2 weeks)
- FPGA Design Cycle
 - Technology-independent optimization (1 week)
 - Technology Mapping (1 week)
 - Placement (1 week)
 - Routing (1 week)
- Coarse-grained Reconfigurable Devices (1.5 week)
- Multi-FPGA Systems (1 week)
- Reconfigurable Computing Applications (2 weeks)
 - Molecular Dynamics
 - Image processing
 - Video processing
 - Bioinformatics
 - Cryptography
 - Fault tolerant systems
- FPGAs vs. Multicore architectures (1 week)
- Advanced Topics: (1.5 weeks)
 - Dynamic Reconfiguration
 - Partial Reconfiguration

Assignments

Homework assignments involve the development and use of CAD tools for reconfigurable computing including [VPR](#) (Versatile Placement and Routing), an academic FPGA place and route system.

Project, Term Paper, Presentation

Semester project will involve 2 phases:

- During the first half of the course, students will:
 - Propose a project on a selected topic taught in class,
 - Document their survey by reporting existing solutions,
 - Tackle a problem and propose their solution,
 - Present their initial findings and solution strategy
- During the second half of the course, students will:
 - Implement their proposed approach,
 - Put together a paper quality document with experimental results,
 - Present project findings

General policies

- Course will have 3-5 assignments, 1 mid-term examination, a semester project
- **NO LATE ASSIGNMENTS WILL BE ACCEPTED**, except under extreme non-academic circumstances discussed with the instructor at least one week before the assignment is due.
- **Make-ups** for assignments and exams *may* be arranged if a student's absence is caused by documented illness or personal emergency. A written explanation (including supporting documentation) must be submitted to your instructor; if the explanation is acceptable, an alternative to the graded activity will be arranged. When possible, make-up arrangements must be completed prior to the scheduled activity.

- Any extenuating circumstances that have an impact on your participation in the course should be discussed with your instructor as soon as those circumstances are known.
- Inquiries about graded material have to be turned in within 3 days of receiving a grade.
- Approximate weight of each assignment will be specified when the assignment is handed out. Assignments will be due in class on the due date.
- The instructor reserves the right to modify course policies, course calendar, assignment values and due dates, as circumstances require.
- Students are strongly encouraged to attend the class. Lecture notes are intended to serve as a supplement and not as a substitute for attending class.
- You are encouraged to discuss the assignment specifications with your instructor and your fellow students. However, anything you submit for grading must be unique and should NOT be a duplicate of another source. The Department of Electrical and Computer Engineering expects all students to adhere to UofA's policies and procedures on Code of Academic Integrity.
<http://web.arizona.edu/~studpubs/policies/cacaint.htm>

Students with Disabilities

If you anticipate the need for reasonable accommodations to meet the requirements of this course, you must register with the Disability Resource Center and request that the DRC send me official notification of your accommodation needs as soon as possible. Please plan to meet with me by appointment or during office hours to discuss accommodations and how my course requirements and activities may impact your ability to fully participate.

Philosophy

"I never did anything by accident, nor did any of my inventions come by accident; they came by work."
Thomas Alva Edison.

- Read before the class
- Participate and ask questions
- Manage your time (3 hours outside class for each credit hour)
- Start working on assignments early

Evaluation

- Midterm: 20%
- Assignments: 20%
- Project: (50% total)
 - 2 Presentations: 10% each
 - Survey paper: 15%
 - Final paper: 15%
- Participation: 10%

Grading Policy

- Overall points $\geq 85\%$: A
- $70\% \leq$ Overall points $< 85\%$: B
- $50\% \leq$ Overall points $< 70\%$: C
- Overall points $< 50\%$: F